REMARKS

Claims 1-19 stand rejected.

35 U.S.C §112, ¶ 1

The Examiner has based a rejection of the Applicants' claims under 35 U.S.C. §112, ¶ 1 on the argument the Applicants' claims fail to meet 35 USC §101. The Examiner has cited In re Kirk, 376 F. 2d 936, 942 (153 USPQ 48, 53) to support the linkage between the argued failure to meet the requirements of 35 U.S.C. §112, ¶ 1 and the failure to meet the requirements of 35 USC §101.

The linkage between 35 U.S.C. §112, ¶ 1 and 35 USC §101 that has been established in In re Kirk and other more recent decisions (See for example, In re Mitchell R. Swartz, 232 F. 3d 862 (Fed Cir. 2000)) is a linkage to the *utility* requirement of the 35 USC §101 not the *statutory subject matter* restriction of 35 USC §101. It is well established in patent law jurisprudence that these are two distinct requirements of the 35 USC §101. In respect to 35 USC §101 the Examiner has rejected the Applicants' claims as failing to read on *statutory subject matter*, not for reciting subject matter (inventions) that lack *utility.* Therefore, rejection under 35 U.S.C. §112, ¶ 1 is not properly founded on a failure to meet 35 USC §101 and for this reason the Applicant submits that a proper prima facie rejection under 35 U.S.C. §112, ¶ 1 has not been made and withdrawal of the rejection under 35 U.S.C. §112, ¶ 1 is requested.

35 U.S.C §101

The Applicant has amended the claims to change "neural network" in the preambles to "electrical neural network". This change is supported by paragraph 27 of the specification. The claims as filed and as amended would be construed by persons of ordinary skill in the art of neural networks to read on an electrical neural network.

The Applicant has not supplied a working model of the invented neural network because this no longer a requirement, however it is useful in considering the §101 issues of the case, to consider what form a working model could take. A working model could and most likely would take the form of a Application Specific Integrated Circuit (ASIC) including circuitry formed in a semiconductor (e.g., silicon) die. The attached paper VLSI Implementation of Programmable Current-Mode Neural Network, by Yasuhiro Ota and Bogdan M. Wilamowski describes the sort of electrical circuits that might be used in a

working model of the Applicants' invention. Note the Applicant has not explicitly recited a semiconductor die in the claims. However more than 50 years since the invention of the integrated circuit, the fact that electronic circuits are typically implemented on semiconductor die's is prosaic and patent claims drawn to electronic circuit that would be implemented in a semiconductor die do not typically recite that the circuits are implemented in a semiconductor die.

In response to the first office action, the Applicant pointed out that a neural network is not, with respect to 35 USC §101, all that different from other "signal processors" such as low-pass filters or demodulators. In the second office action in addressing the Applicants' arguments in respect to the 35 USC §101 the Examiner, quite surprisingly stated:

> "Examiner reminds Applicants that a signal processor, per se, is considered to be no more than a mathematical entity that performs the analysis, interpretation, and manipulation of signals (i.e., functional)." (emphasis added)

The Applicant certainly does not agree that signal processors are no more than mathematical entities. It is with all due candor quite surprising to read such an assertion. Signal processors whether they are analog or more commonly digital are a type of integrated circuit that is widely used in electrical engineering. A market forecast for 2007 estimated a $9 billion market for digital signal processors alone (see http://www.design-reuse.com/news/15714/dsp-chip-market-forecast-grow-moderate-8-2007-according-forward-concepts-study.html). Companies such as Freescale and Texas Instruments sell many different models of Digital Signal Processors (DSPs). Certainly investors in companies making DSP would be shocked to hear that DSPs are no more than mathematical entities. To deny the reality of a signal processors generically or neural networks in particular is to engage in ontological denial. There is no basis to claiming that signal processors are mere "mathematical entities" and as such are excluded under 35 USC §101.

The terms "nodes" and "edges" used in graph theory are particularly suitable for describing generically (without introducing undue limitations on the type circuitry) the structural arrangement of neural networks and the Applicants' has used these terms in the claims but has stated in the specification that in a hardware implementation the nodes and edges can be embodied by electrical circuitry.

In addressing points made by the Applicant in response to the first office action the Examiner states:

"Nodes, edges, weights are clearly recognizable as entities from the theory of directed graphs."

Applicant would like to point out that electrical engineering is a highly mathematical subject and thus it is no surprise at all that mathematical concepts are useful in electrical engineering. For example Laplace transforms are widely used in electrical engineering to describe and analyze linear circuits. Laplace transforms are also presented in numerous claims in issued patents. The Applicant would ask rhetorically: does the fact that Laplace transforms-clearly a mathematical subject are eminently useful and widely used in connection with linear circuits mean that linear circuits are non-statutory subject matter ?—most certainly it does not. By the same token the usefulness of graph theory in the field of neural networks does not taint the field so as to make neural networks non-statutory.

The Examiner also states that:

> "arithmetic operations over nodes, edges, and weights are well known in simple vector-matrix arithmetic."

Be that as it may, it is not at all germane to the neural networks disclosed by the Applicant or the pending claims, because neural networks are necessarily non-linear as opposed to linear and simple vector-matrix arithmetic is insufficient.

The Examiner has stated his agreement with the Applicants' statement that:

> "The utility of neural networks for processing signals is well known to workers in various advanced fields of electrical engineering"

But then stated:

> "However Applicants recite no physical transformation or useful, concrete, and tangible final result in independent claims 1, 4-12 or 13-19. Therefore, Applicants claims a (sic) considered to have no utility."

In re Bilski

As noted above the Examiner has agreed that neural networks have utility, so the issue under 35 U.S.C. to be addressed is whether the claims are drawn to statutory subject matter (whether they define "patent-eligible" subject matter). The recent CAFC case In re Bilski which has substantially refocused the criteria to be applied in judging whether method claims define statutory subject matter under 35 USC §101 is relevant to the Applicants' claims. In re Bilski has put forth two alternative criteria for qualifying under 35 USC §101 which are collectively called the Machine or Transformation test. The former alternative requires that claimed subject matter be tied to a particular machine. The present Applicants'

claims are perhaps an ideal fit to the Machine prong of the test as enunciated in In re Bilski. In the case of the subject matter covered by the Applicants' claims the process steps are intimately connected a particular machine, i.e. electrical neural network. Details of the machine, i.e., neural network are recited in some detail (about half of the independent claims) along with the method steps. The claims recite extensive details of the Machine, i.e., the electrical neural network and then recite method steps which recite various actions and which specifically refer to the recited details of the machine in defining those actions. Thus it is submitted that the Applicants' claims are clearly statutory under the criteria for satisfying 35 USC §101 that has been articulated in In re Bilski.

Comments on Use of Product-by-Process Claims

Applicants' claims 1-12 are product-by-process claims which are infrequently used in electrical cases, however are appropriate in this particular case. There are various prior art training methods for neural networks. Different training methods can produce different final results, e.g., different sets of weights describing the attenuation or amplification factor between nodes. However because it is conventional to represent weights by a factor in the range of zero to one, the claim drafter could not conceive a way to distinguish, in general, the weights produced by the applicants' method and the weights produced by prior art methods hence a product-by-process claiming approach was used.

35 U.S.C §102

The Examiner has rejected claims 1, 4-7, 11, 13, 14, 18 as anticipated by Fahlman et al. "The Cascade-Correlation Learning Architecture", 1990. The method described by Fahlman et al is clearly quite different from that recited in Applicants' independent claims 1 & 13. Fahlman describes a method according to which hidden nodes are added one at a time, and before their outputs are connected to the output nodes of the neural network, the input weights of the newly added hidden nodes are trained to maximize the magnitude of the correlation between their output and the output of neural network itself. After this correlation is maximized, the input weights are frozen and the outputs of newly added nodes (which are connected to output nodes), are connected and the connections between the newly added nodes and the output nodes of the network are re-trained. Thus, Fahlman's training never has to contend with training an edge weight that is multiple layers deep in a network. In summary, because of this latter point claims 1 & 13 do not read on the methods disclosed by Fahlman. Specifically, Fahlman does not

disclose:

> "for each particular node of the plurality of additional nodes between said second node and said output node, computing an additional summand by multiplying together the first factor, a weight characterizing one of the first plurality of directed edges that couples the second node to the particular node, a weight characterizing one of the second plurality of directed edges that couples the particular node to the output node, and a value of a transfer function of the particular node"

as recited in independent claims 1 & 13. The Examiner himself quoted a relevant portion of Fahlman which states "Once again we are only training a single layer of weights". For, at least, the foregoing reasons claims 1, 4-7, 11, 13, 14, 18 are not anticipated by Fahlman and withdrawal of the rejection over Fahlman is requested.

Claim 11 & 18 depend from claims 10 and 17 respectively however the Examiner did not address the limitations of claims 10 & 17 in making the rejections of claims 11 & 18 under 35 U.S.C §102 therefore it is submitted that a proper prima facie rejection under 35 U.S.C §102 has not been made.

35 U.S.C §103

Claim 2 was rejected under 35 U.S.C §103(a) over Fahlman in view of Mashiko (U.S.P. 5,202,956). Claim 2 depends from claim 1 and includes all the limitations thereof. For the reasons set forth above in respect to claim 1 it is submitted that claim 2 is allowable.

Claim 3 was rejected under 35 U.S.C §103(a) over Fahlman in view of Smyth (U.S.P. 6,092,058). The portion of Smyth pointed to by the examiner concerns an autoregressive filter not a neural network. Whereas the attenuators are used in feedback loops of the autoregressive filter disclosed by Smyth neural networks such as those disclosed by the applicant do not include any feedback pathways. In any case claim 3 depends from claim 1 and includes all the limitations thereof. For the reasons set forth above in respect to claim 1 it is submitted that claim 3 is allowable.

Parenthetically, regarding 35 U.S.C §101 the Applicant would draw the Examiner's attention to the equivalence drawn between mathematical entities "linear expansion coefficients" and circuit characteristics "the attenuations of the circuit model" pointed out by Smyth in the text portion quoted by the Examiner, the point being the fact that circuit functions are often described in mathematical terms by practicing engineers.

Claims 8 & 15 were rejected under 35 U.S.C §103(a) over Fahlman in view of Watrous "Learning

Algorithms for Connectionists Networks: Applied Gradient Methods of Nonlinear Optimization", 1988. Claims 8 & 15 depend from claims 1 & 13 respectively and include all the limitations thereof. For the reasons set forth above in respect to claims 1 & 13 it is submitted that claims 8 & 15 are allowable.

Respectfully submitted,

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